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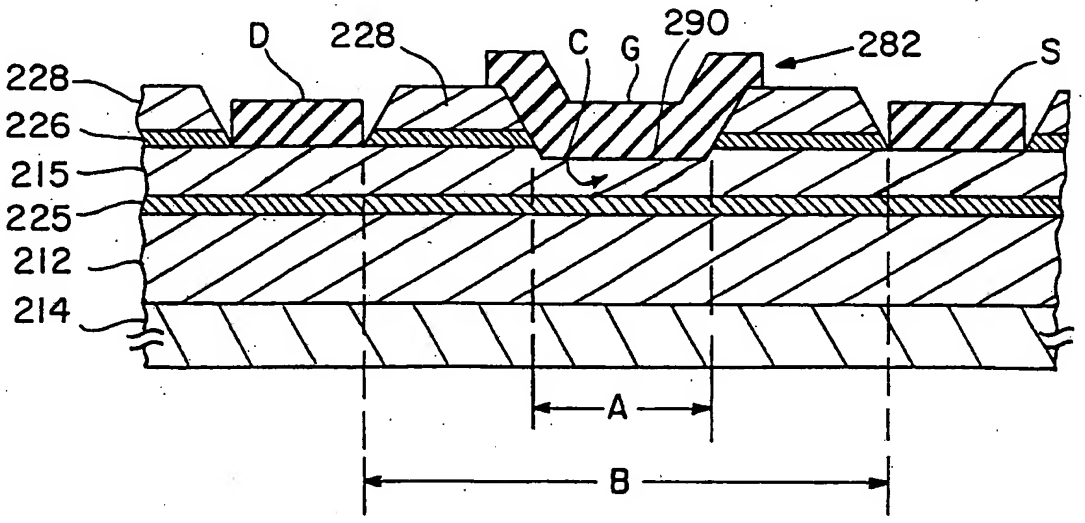

(57) Abstract

A new III-V buffer or passivation material is described which is produced by low temperature growth (LTG) of III-V compounds. The material has unique and desirable properties, particularly for closely spaced, submicron gate length active III-V semiconductor FET devices, such as HEMT's, MESFET's and MISFET's. The LTG material is grown under ambient conditions which incorporate an excess of the more volatile of the III-V species into the grown material. The new material is crystalline, highly resistive, relatively insensitive to light, and can be overgrown with high quality III-V active layers or used as a passivation material to insulate and protect active device structures.

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III-V BASED INTEGRATED TRANSISTOR

Background Art

Semiconductor compounds of the III-V materials and alloys thereof; such as the compounds gallium arsenide (GaAs) and indium phosphide (InP) and the alloy aluminum gallium arsenide (AlGaAs) have unusual optoelectronic properties which make them attractive for many applications; ranging from microwave devices to optoelectronic devices. Among these applications is the use of such materials to make devices for high-speed logic integrated circuits and for microwave integrated circuits. The Schottky-barrier gate metal-semiconductor-field-effect transistor (MESFET) is a typical device used in these integrated logic circuits.

The MESFET is a three terminal device consisting of a source, gate and drain. The source and drain terminals form low resistance contacts to a channel whose conduction is controlled by the depletion field of a Schottky-barrier gate. The conducting channel, which is placed on a semi-insulating (SI) substrate, may be formed either by ion implantation into the semi-insulating material, or by epitaxially growing the active layer on semi-insulating material.

A number of problems associate with MESFET devices and circuits are attributed to the SI substrate. Such problems include backgating (or sidegating), hysteresis in the dependence of the drain-source current I_{ds} upon drain-source voltage V_{ds}, light sensitivity, low output resistance R_d, low source-drain breakdown voltage BV_{SD}, and low output power gain at RF frequencies. Among these problems, backgating is the most significant for both digital and analog circuit applications.

In addition to these problems, increased subthreshold

problems, backgating is the most significant for both digital and analog circuit applications.

In addition to these problems, increased subthreshold leakage current, threshold voltage shifts, and the inability to fully pinch-off the device for large V_{ds} can occur as the gate length of MESFET's is reduced to submicron dimensions. Also, R_d and BV_{SD} are further decreased as the gate length is reduced. These problems are called short-channel effects and the characteristics of the layer underlying the active region can have a profound influence on them.

Backgating or sidegating is the change of I_{ds} in a MESFET as a result of a voltage applied to the substrate or an adjacent, and nominally isolated, contact pad (sidegate). Even though the sidegate and MESFET may be physically separated, as by mesa etching, the interaction may still arise because the substrate is of finite resistivity and charge can accumulate at the interface between the active layer and the substrate. In response to changes in voltage on the substrate or adjacent devices, the substrate conducts enough current to modulate the interface space-charge region. When this interfacial depletion region widens into the active channel, the device current is reduced.

A buffer layer is often inserted between the active layer and the substrate to alleviate the problem of backgating. To reduce backgating and other substrate related effects, the buffer layer should provide an increase in bulk resistivity. A number of possible buffer layers have been suggested, including undoped GaAs,

AlGaAs, and superlattice (GaAs/AlGaAs) buffers. Heretofore such buffer layers have met with only limited success.

Another device useful for high-speed circuits is the MISFET (metal-insulator-semiconductor-field-effect-transistor). This, like the MESFET is a three terminal device. In the MISFET an insulator layer is formed between the underlying active channel region and the gate. In III-V devices it has been difficult to develop an insulator which meets all the requirements for such a layer.

Disclosure of the Invention

The invention comprises a layer of III-V material, or an alloy thereof, and a process for growing such a layer on a substrate by molecular beam epitaxy (MBE) at low substrate temperatures. The low-temperature-grown (LTG) layer thus grown is optically inert or inactive, that is, the electrical conductivity of the material is relatively insensitive to light and the material is substantially non-luminescent. Furthermore, the layer is electrically insulating. The layer is especially useful as a buffer layer for growth of III-V MESFET's, MOSFETs or MISFETs thereon or as an insulator layer for MISFETs and as a passivation layer for MESFETs or other FETs.

After the LTG layer is grown to a suitable thickness, the outer surface is reconstructed and stabilized to enable good quality crystal growth of subsequent layers. Reconstruction is achieved by annealing in an ambient containing the more volatile of the III-V species, i.e., for GaAs the ambient is As; for InP the ambient is P. The

function of stabilization is to prevent or minimize out-diffusion of the more volatile specie from the low temperature buffer layer. This may be achieved by providing a careful choice of initial regrowth temperature, to produce a buffer stabilizing layer over the low temperature buffer layer. Alternatively, a buffer stabilizing layer of material, which is capable of preventing out-diffusion, may be grown over the LTG layer.

Brief Description of the Drawings

Fig. 1 is a schematic cross-section of GaAs MESFET and backgate terminal formed on a buffer layer of the invention.

Fig. 2 is a plot of normalized saturated drain source current (I_{DSS}) versus backgating voltage for GaAs MESFET's fabricated in accordance with the invention (curves a and b) and GaAs MESFET's fabricated using prior art techniques (curves c-f).

Fig. 3 is a schematic cross-section of an alternate embodiment of the invention in which a GaAs device is formed on a buffer layer of the invention, which layer is formed over a silicon substrate.

Fig. 4 is a schematic cross-section of another embodiment of the invention in which an optical device and an electronic device are monolithically combined using the buffer layer of the invention for vertical optoelectronic isolation.

Fig. 5 is a schematic cross-section of a metal-insulator-semiconductor-field-effect-transistor (MISFET) embodiment of the invention in which an LTG layer forms the insulator layer for the gate of a MISFET device.

Fig. 6 is a schematic cross-section of an alternate embodiment of the invention in which the source and drain edges of the metal gate of a III-V MESFET overlap a LTG insulation layer.

Fig. 7 is a plot of drain-source current (I_{ds}) versus drain-source voltage (V_{ds}) for the device of Fig. 6.

Best Mode of Carrying Out the Invention

I. GaAs MESFET EMBODIMENT

Referring now to Fig. 1, the invention will be described in detail in connection therewith. It should be understood that while the device of Fig. 1 is a GaAs MESFET structure, other devices and other III-V materials are contemplated as being within the scope of the invention. Fig. 1 is a schematic cross-section of a GaAs MESFET structure 10 made in accordance with the invention to include a new buffer layer 12 and buffer stabilizing layer 23.

Note: While the term "layer" is used to define the films formed on substrates, it is intended that this term also covers films disposed in regions of the substrate other than the entire substrate surface.

Buffer layer 12 is formed by MBE on a SI-GaAs substrate using Ga and As_4 beam fluxes, under arsenic stable growth conditions, at optimal substrate temperatures between 150 to 250°C, and at growth rates of 1 micron/hour.

The range of 150-250°C is believed to be an optimal growth temperature range to produce the buffer layer 12. However, temperatures below 300°C are contemplated as being suitable for buffer layer growth. These growth

temperatures are substantially lower than those used in previous studies of GaAs grown by MBE at a low substrate temperatures ["Growth-Parameter Dependence of Deep Levels in Molecular-Beam-Epitaxial GaAs", Stall et al., Electronics Letters, (1980) 171-172; "Growth Temperature Dependence in Molecular Beam Epitaxy of Gallium Arsenide", Murotani et al., Journal of Crystal Growth 45 (1978) 302-308; "Temperature Range for Growth of Autoepitaxial GaAs Films by MBE", Neave et al., Journal of Crystal Growth 43 (1978) 204-208; "An Investigation of GaAs Films Grown by MBE at Low Substrate Temperatures and Growth Rates", Metze et al., J. Vac. Sci. Technol. B1(2), (1980) 166-169].

The reflected high energy electron diffraction (RHEED) pattern observed during growth, for substrate temperatures as low as 200°C, indicates that the buffer is crystalline. This result has been confirmed by double-crystal x-ray diffraction. The buffer layer resistivity increases with decreasing growth temperature, but below 200°C it has not sufficient thickness. All the data presented here are for buffers grown at 200°C. The resistivity of the buffer layers grown is 10^7 ohm-cm. The exact resistivity could not be determined using conventional Hall-effect measurement techniques, because the resistivity exceeds the measuring capability of our equipment. The material is non-stoichiometric GaAs having an excess of about 1% As, as determined by Auger Electron Spectroscopy.

After a buffer layer 12 of about 2 microns is grown as described above, on an SI-GaAs substrate, the structure is brought to a temperature of between about 480 and 580°C

and heat treated in an arsenic ambient at that temperature for about 10 minutes to reconstruct the exposed surface 25 of layer 12 to a short depth illustrated by the dotted line L1. Next, a thin (30-200Å) buffer stabilizing layer 23 of GaAs is deposited by MBE at a relatively low growth temperature of 550°C or less. The heat treatment appears to alleviate surface crystalline defects and the stabilizing layer 23. As an alternative to regrowth of the GaAs, other materials capable of preventing out-diffusion, but having appropriate lattice matching feature for growth of active layer thereon, may be used, such as, Al, AlGaAs, or a thin GaAs/AlGaAs superlattice.

An 0.3 micron thick n-doped GaAs layer is then grown by MBE on layer 23 at typical MBE GaAs growth temperature of 600°C. MESFET's 16 were then fabricated on the doped GaAs layer by conventional etching and metallization processes.

For experimental purposes, in order to demonstrate backgating performance, a sidegate 22 was formed adjacent to MESFET 16 and mesa-isolated by etching up to, or into, the top surface 25 of buffer layer 12.

MESFET 16 consists of an n+ source region S and an n+ drain region D, laterally separated by an n-channel region C formed beneath a (Schottky) metal gate electrode G. Ohmic contacts 18 of Ni/Ge/Au or Pd/Ge/Au are formed on the source and drain regions. The gate electrode G is formed of Ti/Au.

The measured gate length, gate width, and source-drain spacing of this experimental device are 2, 98, and 5.5 microns, respectively. An ohmic contact 22, isolated from the MESFET 16 by mesa etching, served as the sidegate. For comparative purposes, MESFET's, as

described above, were fabricated in MBE n-GaAs layers grown upon the buffer stabilizing layer 23 of the invention and also upon buffer layers of undoped GaAs, AlGaAs, and GaAs/AlGaAs superlattices. All the buffer layers were grown by MBE and were 2 microns thick. In each case, the active layer 15 was doped to approximately $2x10^{17}$ cm^{-3} with silicon and was 0.3 microns thick. MESFET's were also fabricated in commercial vapor phase epitaxy (VPE) n-GaAs layers deposited on semi-insulating GaAs substrates and on layers made by direct ion implantation into the SI GaAS substrates. The gate recess depth is roughly half the active layer thickness, and mesa etching was used to isolate the devices.

The most dramatic improvement in device performance provided by the new buffer layer is the elimination of backgating, as illustrated by Fig. 2. Fig. 2 is a plot of normalized I_{dss} $[I_{dss}(V_{BG})/I_{dss}(0)]$ plotted versus applied backgating voltage V_{BG}. A sidegate 22 spaced 50 microns from the MESFET 16 and a drain to source voltage of 2.5 V are used. Data obtained both in the dark (solid line) and in white light (dotted line) are shown. The lines in the figure are included only as a convenience in visualizing the data.

The data in Fig. 2 provides a comparison between backgating in MESFET's fabricated in active layers on the new buffer 12 (curves a and b) with backgating in MESFET's fabricated in active layers on an undoped GaAs buffer (curves e and f) and on an undoped GaAs/$Al_{0.45}Ga_{0.55}As$ superlattice buffer grown by MBE at 700°C (curves c and d). Both GaAs and superlattice buffered devices show

backgating and light sensitivity, while the device with the new buffer shows neither. Although not shown here, MESFET's fabricated using all of the other buffers show light sensitivity and backgating. Of the alternative buffers, the AlGaAs and superlattice buffers grown at 700°C appear to be the best.

Although the data presented in Fig. 2 were measured using a sidegate spaced 50 microns from the MESFET 16, a sidegate spaced 15 microns from the MESFET was also used. For -50 V applied to the sidegate and V_{ds} = 2.5 V, the new buffered device still showed no backgating. For the same voltages, I_{dss} of the superlattice buffered MESFET was reduced by 50% and the GaAs buffered devices destructively broke down.

Although grown from Ga and As beam fluxes, the new buffer 12 differs markedly from GaAs grown at normal growth temperatures of approximately 600°C. In addition to its larger resistivity, the grown surface is not reconstructed, as indicated by the photoluminescence (PL) spectrum. However, doped layers of GaAs grown by MBE upon the buffer stabilizing layer 23 are of comparable optical and electrical quality to similar layers grown upon conventional undoped GaAs buffers grown by MBE at 580°C. The PL spectra for the doped films on the new buffer capped by stabilizing layer 23 are essentially identical to those for the doped films on the conventional undoped GaAs buffer.

The new low temperature buffer layer 12 is capable of substantially eliminating radiation transient effects in III-V integrated circuits. The mechanism of transient radiation related failure in III-V circuits is believed to be caused by diffusion of hole-electron pairs that have

been generated in the bulk of the III-V substrate by the radiation, into the active region of the devices fabricated on the surface of the substrate. Because of the optoelectronic inertness and insulating characteristics of the new III-V buffer layer, it should eliminate the undesirable effects of radiation on circuit performance. Not only should the buffer itself not be susceptible to the radiation, but the charge carriers generated in the semi-insulating III-V substrate should be blocked from entering the active region of the device by the presence of the intervening buffer layer.

Recent measurements of the GaAs MESFET devices incorporating the new MBE low temperature buffer layer indicate that the new MBE low temperature buffer layer does, indeed, substantially reduce the sensitivity of MESFET devices to pulsed ionizing radiation. Transient radiation measurements were made on a MESFET device with an undoped GaAs buffer layer and on a MESFET device with the new MBE buffer layer. The MESFET with the new MBE low temperature buffer layer showed an overall several order of magnitude reduction in sensitivity to pulsed ionizing radiation as compared with the MESFET with the undoped GaAs buffer layer.

II. GaAs ON Si HIGH ELECTRON MOBILITY TRANSISTOR (HEMT) EMBODIMENT

Fig. 3 is a cross-sectional view of an alternate embodiment of the invention, wherein a HEMT device 56 is formed on the buffer stabilization layer 33.

Layer 33, the buffer stabilizing layer, is formed by MBE, as in the Fig. 1 embodiment, on a low temperature MBE

GaAS buffer 32. Unlike Fig. 1, the GaAs buffer 32 is formed over a silicon (Si) substrate 34, with an adjusting lattice layer of GaAs 36 sandwiched between to serve as a growth stabilizing layer. The use of the Si substrate has the advantage that Si devices may be formed on laterally adjacent isolated regions of the surface of substrate 34 and conductively coupled by suitable metallization to the GaAs HEMT device 56, thus providing a GaAs/Si monolithic integrated structure, wherein the electro-optical properties of the GaAs material may be conveniently combined with the electronic properties of the Si material. A suitable isolation technique is proton bombardment of the active layers 38 and 40 down to the stabilizing or buffer layers 33 and 32 laterally adjacent the device 56 to convert the volume bombarded to semi-insulating material. Alternatively, mesa etching, as in Fig. 3, can be used for isolation.

After LTG GaAs buffer layer 32 is formed, the upper surface is reconstructed and a stabilizing layer 33 is formed, as previously described. Next, a GaAs/AlGaAs HEMT device is formed on the stabilizing layer by MBE deposition of an undoped low bandgap GaAs layer 38, followed by MBE deposition of an n+ modulation doped higher bandgap AlGaAs layer 40. At the interface between the two layers 38 and 40, a two dimensional electron gas is formed, which contributes to the high electron mobility of the HEMT device (See "Gallium Arsenide Technology", Howard W. Sams & Co. 1985, Chapter 4, pp 107-153 for a more detailed discussion of HEMT's). Suitable ohmic drain D and source S contacts are evaporated onto the AlGaAs layer 40 with a Schottky-barrier type electrode G being

formed between the two in the well-known manner. It should be noted that while the GaAs HEMT device 56 is shown for illustrative purposes in Fig. 3, any III-V compound device which can be grown on GaAs is intended to be included in this embodiment. One example is a pseudomorphic InGaAs/AlGaAs HEMT.

III. OPTOELECTRONIC DEVICE

The essentially zero electrical conductivity, and the largely optically inert properties of the new low temperature buffer material, may be advantageously utilized in the formation of an integrated optoelectronic circuit. Such a circuit will now be described in connection with Fig. 4. In the embodiment of Fig. 4, a GaAs/AlGaAs double heterostructure epitaxial laser region 66 is formed by conventional techniques, i.e., liquid phase epitaxy (LPE) or MBE, on a GaAs substrate 64. A low temperature buffer layer 62, with a reconstructed surface 65 and a buffer stabilizing layer 63, is then formed as in the previously described embodiments. This optically inert/non-conductive buffer serves as a vertical isolation layer. Next, an n-GaAs FET layer 80 is formed on the stabilizing layer 63.

In the region where the laser is formed, the layers 80, 63, 65, and 62 are removed, as by etching, and proton bombardment applied to the underlying structure, to form a lateral isolation region 72. An insulating layer 68 of, for example, SiO_2, or polyimide, is then formed over the top surface. The layer 68 is etched away in regions where the laser contact 74 and drain D and source S contacts for

the MESFET 82 are to be formed.

Appropriate metallization/doping is applied to the regions of the openings to form the contacts and further openings in the oxide 68 are formed and the FET layer 80 recessed. Gate contact G is formed through an additional insulating mask region 84. Metallization 70 is applied over layer 68 to interconnect MESFET 82 to laser contact 74. A suitable contact 76 is then formed on substrate 64. (See T. Fukuzawa, et al., "Monolithic Integration of GaAlAS Injection Laser with a Schottky-gate Field Effect Transistor", Appl. Phy. Lett. Vol. 36, pp. 181-183, (1980) and N. Baz-Chaim, et al., "GaAs Integrated Optoelectronics", IEEE Trans. on Electron. Devices, Vol. ED-29, pp. 1372-1381, 1982 for a description of conventional process steps for MESFET and laser integration.)

The laser may be optionally formed as a two dimensional array of surface-emitting diode lasers, as described in J.P. Donnelly, et al., "Monolithic Two-Dimensional Surface-Emitting Arrays of GaAs/AlGaAs Diode Lasers", Appl. Phys. Lett., Vol. 51, pp. 1138-1140, 1987.

IV. MISFET DEVICE

The ability to fabricate silicon MOSFET devices (metal-oxide-semiconductor-field-effect-transistors) has made possible NMOS and CMOS very large scale integration (VLSI) technology, the workhorses of today's computers and electronics. Heretofore, GaAs MOSFET or MISFET (metal-insulator-semiconductor-field-effect-transistors) devices have not been possible, because the oxide or insulator pins the GaAs Fermi level at the surface due to a large

density of interface states. Considerable effort has been undertaken to develop an insulating layer that does not pin the GaAs Fermi level at the surface. To date, these efforts have not met with commercial success. In the embodiment of Fig. 5, a GaAs MISFET is shown which has a number of advantages relative to GaAs MESFET's. Some of these advantages relative to GaAs MESFET's are: reduced gate current, more uniform and larger threshold voltage, larger logic voltage swings, and the possibility of making complementary III-V MISFET integrated circuits.

We have fabricated n-channel depletion-mode GaAs MISFET's and MIS capacitors using the new low temperature buffer as the gate insulator. A GaAs MISFET structure is illustrated in Fig. 5. The substrate 114, buffer 112, annealed region of the buffer 125, stabilization layer 123, and the active FET layer 115, are the same as for the MESFET of Fig. 1, previously described. On top of the active layer 115, a thin layer 128 of the low temperature buffer (50-1000Å) is formed, as previously described, with an annealed restructured region and stabilizing layer (not shown). A GaAs gate layer 130 (50-250Å thick) is then deposited by MBE over the gate buffer layer 128. The gate metal G is deposited on the upper GaAs gate layer 130. Regions of the upper GaAs layer 130 and the upper buffer layer 128 are removed laterally adjacent the gate region and ohmic contacts D and S, for the drain and source, respectively, are fabricated in these regions on the active FET layer 115. Either Mesa isolation, or proton bombardment, is used to isolate the individual devices 182.

MISFET I-V (current-voltage) characteristics of an experimental device, fabricated as above, show that the channel region beneath gate G can be fully pinched-off and the MIS C-V (capacitance-voltage) characteristics show a low interface state density. This device has not yet been optimized, although the preliminary results are encouraging. Alternative layers to the top thin GaAs gate layer 130 include thin layers of AlGaAs, thin insulating layers, such as silicon dioxide or silicon nitride, or thin composite layers of these materials. The MISFET depicted in Fig. 5 is an n-channel, depletion mode device. It is expected that n-channel and p-channel depletion, enhancement, and inversion mode GaAs MISFET devices may be possible using the new low temperature buffer layer as the gate insulator.

V. MESFET WITH OVERLAPPING MIS GATE STRUCTURE

Since the highest field occurs at the drain side of the gate edge of a MESFET, it is possible that a high gate-breakdown voltage can still be achieved even if an MIS structure is formed only at the edge of the MESFET gate as shown in Fig. 6. The GaAs MESFET 282 of Fig. 6 with an overlapping-gate structure has a breakdown voltage substantially higher than that of a conventional MESFET. The bottom of the Schottky-barrier gate G contacts the channel region 290 as in a conventional MESFET, but both gate edges rest on LTG GaAs insulation or passivation layer 228. This structure has the advantage that parameters such as drain current and transconductance g_m are not adversely affected, and, in addition, it can be

applied to other devices such as the high-electron-mobility transistor (HEMT) of Fig. 3.

As shown in the schematic cross-section of Fig. 6 epitaxial layers, similar to those used for the LTG GaAs MISFET of Fig. 5, were grown by molecular beam epitaxy on a semi-insulating GaAs substrate 214. The layers consist of a 2000-Å-thick LTG GaAs buffer layer 212, a 100-Å-thick AlAs stabilizing layer 225, a 1000-Å-thick GaAs active layer 215 doped with Si to 4 x 10^{17} cm^{-3}, a 100-Å-thick AlAs stabilizing layer 226, and a 2000-Å-thick LTG GaAs layer 228. The growth temperature was 190°C for the LTG GaAs layers and 580°C for all other layers.

For comparison purposes, conventional-gate and overlapping-gate MESFET's were fabricated on respective wafers having this layer structure. Ohmic contacts D, G and S were formed by first etching through the top LTG GaAs and AlAs layers 228 and 226 and then depositing Ni/Ge/Au contact pads D, G and S directly on the conducting-GaAs layer 215.

On the wafer used for the MESFET with a conventional gate structure (not shown), the gate area was first defined by photoresist. The LTG GaAs and AlAs layers were then etched away in the gate opening and the conducting GaAs channel was recessed to obtain a drain saturation current I_{dss} of 200 ma/mm of gate width. Next, Ti/Au was evaporated and the gate was formed by a liftoff of the photoresist pattern.

On the wafer used for the overlapping-gate structure of Fig. 6, the same gate mask as used above was used to define an opening for the removal of the LTG GaAs and AlAS

layers and for the channel-recess etch (again to an I_{dss} value of 200 ma/mm). This resist layer was removed after etching. A wider gate opening that overlaps the gate-recess region and the LTG GaAs top layer 228 near the edges of the recess region was defined for the gate liftoff using a second layer of photoresist. The gate-recess length (A), drain-source spacing (B), and gate width (length of device perpendicular to plane shown) were 1.5, 6, and 250 μm, respectively. Proton implantation was used for device isolation. The width of the gate overlap is less than 0.3 μm on either side of the gate recess, although in principle, this overlap preferably can be considerably smaller. In one area on this wafer, the LTG GaAs layer 228 and the AlAs layers 226 in the gate region were not etched, allowing MISFET's similar to those described in Fig. 5 to be fabricated on the same wafer with the overlapping-gate MESFET's.

The I_{ds}-V_{ds} characteristics of the overlapping-gate MESFET are shown in Fig. 7. Note that curves A-E were taken in the 80 μs pulse mode of the curve tracer to reduce the heat generated by the device. The curves differ in accordance with the applied voltage. Near pinch off, there is no noticeable excessive drain current for V_{ds} as high as 35 V. The g_m values are 120 and 136 mS/mm for the conventional-gate and the overlapping-gate MESFET's of Fig. 6, respectively. The higher g_m for the overlapping-gate MESFET may be due to the differences in gate structure or may be simply due to the difference in series resistance caused by processing-related variations in ohmic contacts and gate-source spacing. The scattering

(S) parameters of these MESFET's were measured with V_{ds} = 6 V and V_{gs} = 0 V. The unity-current-gain frequency f_T derived from measured S parameters is 4.8 GHz for the overlapping-gate MESFET and 5.3 Ghz for the conventional-gate MESFET, while the values of maximum frequency of oscillation f_{max} are 15.2 and 14.4 Ghz for the overlapping-gate and conventional-gate MESFET's, respectively.

The breakdown voltages for the different devices are listed in Table I below:

TABLE I

Breakdown Voltages for FET's

	LTG-GaAs-PASSIVATED MESFET WITHOUT GATE OVERLAP	LTG-GaAs-PASSIVATED MESFET WITHOUT GATE OVERLAP	LTG GaAs MISFET
GATE-DRAIN BREAKDOWN (V)	25	42	45
DRAIN-SOURCE BREAKDOWN (V)	22	35	37

The gate-drain breakdown voltage, defined at 200 μA/mm gate current, is 25 V for the conventional-gate MESFET and 42 V for the overlapping-gate MESFET. At pinch off, the drain-source breakdown voltage for the conventional-gate and overlapping-gate MESFET's is 22 and 35 V, respectively. In contrast, the breakdown voltages for a standard MESFET fabricated with this same mask set but without an LTG GaAs passivation layer are 10 V for the drain-source breakdown and 15 V for the gate-drain breakdown.

The characteristics of the LTG GaAs MISFET on the second wafer are similar to those reported previously [C.L. Chen, et al., IEEE Electron Device Lett., 12,306 (1991)]. The forward gate turn-on voltage, also defined at 200 μA/mm of gate current, is 4.5 V for the MISFET compared to 0.4 V for the MESFET on the same wafer. The gate-drain breakdown voltage and drain-source breakdown voltage at pinch off for the MISFET are 45 and 37 V, respectively.

The breakdown voltage of the new MESFET of Fig. 6 has been enhanced significantly by the use of overlapping-gate structure. Although the gate has a Schottky contact to the conducting channel, the breakdown voltages are nearly equal to those of the MISFET, in which the entire gate metallization rests on a high-resistivity LTG GaAs layer. It appears that the high-resistivity LTG GaAs layer under the overlapping portion of the gate in the new MESFET has altered the electric field distribution. As a result, the components of the two-dimensional field that are believed to be responsible for the breakdown are significantly reduced by the new structure. It is important for the success of this approach that the material under the edges of the overlapped-gate have a high resistivity and that the Fermi level at the interface between this material and the conducting channel is not pinned by interface-state charge. Both of these criteria are met by the LTG GaAs material of layer 228, whereas dielectric passivants like SiO_2 and Si_3N_4 generally fail to meet the second condition.

The slightly higher breakdown voltage in the MISFET is due to the added dielectric-breakdown voltage of the

LTG GaAs gate-insulator layer itself. The results suggest that the majority of the increase in breakdown voltage observed for LTG GaAs MISFET's can be attributed to just a small portion of the MIS gate structure near the edges.

A substantial increase in the breakdown voltage of a GaAs MESFET has been achieved by using an LTG GaAs surface passivation layer and a metal gate that overlaps the LTG GaAs layer at the edges of the gate. This increase in breakdown voltage was obtained without sacrificing drain current or gain. The breakdown voltage of such a MESFET is approximately equal to that of the LTG GaAs MISFET minus the gate forward turn-on voltage of the MISFET, this latter value being dominated by the dielectric-breakdown voltage of the LTG GaAs gate insulator. The overlapping-gate approach can be applied to any MESFET-like device, such as a HEMT, without interfering with the device active-layer structure. In addition to improving the breakdown voltage, the same LTG GaAs layer could also eliminate the need for further dielectric passivation.

Equivalents

Those skilled in the art may recognize other equivalents to the specific embodiments described herein, which equivalents are intended to be encompassed by the claims attached hereto. For example, other combinations of III-V materials are contemplated for use as low temperature buffer layers, stabilizing layers, and active layers.

The table below lists various combinations of III-V materials in column 1 versus normal or typical MBE substrate growth temperatures in column 2, approximate

recommended substrate growth temperatures for the MBE buffer layer in column 3, and approximate recommended substrate growth temperatures for the stabilizing layer in column 4.

TABLE

1	2	3	4
GaAs	580°C	150-300°C	300-550°C
GaP	550°C	150-300°C	350-500°C
InP	450°C	50-200°C	350-450°C
AlGaAs	680°C	150-450°C	500-600°C
InGaAs	500°C	50-300°C	300-500°C

CLAIMS

1. A method of making an active III-V device comprising the steps of:

a) forming a first layer of insulative III-V material by deposition of III and V materials on a substrate at a predetermined growth temperature below 450°C;

b) subjecting said first layer to a heat treatment at a temperature above the growth temperature in an ambient containing the more volatile of said III-V materials to provide an excess of the more volatile material in said intermediary layer;

c) forming a second layer of epitaxial III-V material on or over said first layer at a predetermined growth temperature above 450°C;

d) forming a third layer of insulative III-V material on, or over, said second layer by deposition of III and V materials at a predetermined growth temperature below 450°C followed by a heat treatment at a temperature above the growth temperature in an ambient containing the more volatile of said III-V materials to provide an excess of the more volatile material in said intermediary layer; and

e) forming source, drain and gate regions in the second layer wherein the gate region is insulated from the source and drain regions by the material of the third layer.

2. The method of Claim 1 wherein the substrate is formed of silicon with an adjusting lattice layer disposed between the first and the second layer.

3. The method of Claim 1 wherein the material of the first, second and third layers comprise GaAs.

4. A semiconductor structure comprising:
   a) a substrate;
   b) a first layer of highly resistive III-V material on the substrate for reducing side-gating or back-gating effects in the semiconductor structure, and wherein one of the III-V materials is more volatile than the other and wherein the first layer contains an excess of said more volatile material;
   c) an epitaxial device layer of III-V material formed on, or over, the first layer; and
   d) a second layer of highly reactive III-V material formed on the device layer and wherein one of the III-V materials is more volatile than the other and wherein the second layer contains an excess of said more volatile material;
   e) a semiconductor device having device elements formed in the device layer and wherein device elements are isolated from one another by the material in said second layer.

5. The structure of Claim 4 wherein the III-V material is selected from the group comprising GaAs, GaP, InP,

AlGaAs or InGaAs.

6. The structure of Claim 4 wherein the device comprises an FET with source, drain and gate elements and wherein said second layer of said highly resistive III-V material extends laterally between the gate element and the drain and source element.

7. The structure of Claim 4 wherein the device comprises an FET and the elements comprise drain, source and gate electrodes contacting the device layer and wherein the gate electrode is electrically insulated from the drain and source electrodes by portions of the highly resistive III-V material of the second layer.

8. The structure of Claim 4 in which the III-V material is GaAs and the more volatile material is As.

9. The structure of Claim 7 wherein the second gate electrode extends over portions of the layer of highly resistive III-V material.

10. The structure of Claim 4 wherein a monolithically integrated device taken from the group comprising lasers, photoconductors and FET's is formed laterally adjacent on a substrate in common with said semiconductor device and vertically isolated therefrom by said first layer and horizontally isolated by said second layer.

11. The structure of Claim 4 in which the substrate is a semi-insulator.

12. The method of Claim 1 wherein the excess is in the order of 1%.

13. The method of Claim 1 wherein the III-V material is GaAs, the more volatile material is As, and the excess of As is in the order of 1%.

14. The method of Claim 1 wherein the III materials comprise one, or more, of the elements Al, Ga In and the V materials comprise one or more of the elements P, As or Sb.

15. The method of Claim 1 wherein the first and third layers are formed by MBE of AlGaAs, InP, GaP, GaAs, or InGaAs.

16. The method of Claim 1 wherein the first and third layers are formed of InGaAs.

17. A field-effect transistor device comprising:

a) a substrate;

b) a device layer formed over the substrate;

c) a transistor formed in the device layer, said transistor having a gate electrode overlying and in contact with a channel region in the device layer and source and drain electrodes laterally displaced from said gate electrode and insulated therefrom by a resistive III-V material formed

over said device layer and wherein the III-V material consists of one element which is more volatile than another element and which is formed at a temperature and an ambient environment in which an excess of the more volatile element is incorporated into the III-V material.

18. The device of Claim 17 in which the gate electrode extends laterally over said III-V material.

19. The device of Claim 17 further including a buffer layer of III-V material formed between said substrate and said device layer.

20. The device of Claim 17 wherein the III-V material is taken from the group comprising GaAs, AlGaAs, InGaAs, InP or GaP.

21. A method of forming a field-effect transistor device comprising the steps of:

a) forming a device layer over a substrate;

b) forming a transistor in the device layer having a gate electrode disposed over a channel region and in contact with the device layer with source and drain electrodes disposed laterally adjacent the gate electrode; and

c) forming an insulative region of III-V material laterally between the gate electrode and the drain and source electrodes, such region being formed by deposition of group III and group V

specie at a growth temperature below 450°C, followed by heat treatment of the deposited specie in an ambient containing the more volatile of said specie to incorporate an excess of said more volatile specie in said III-V material.

22. The method of Claim 21 wherein the gate electrode extends laterally over the insulative region.

23. The method of Claim 21 wherein the group III-V material is formed by MBE of material from the group comprising GaAs, InGaAs, AlGaAs, GaP and InP.

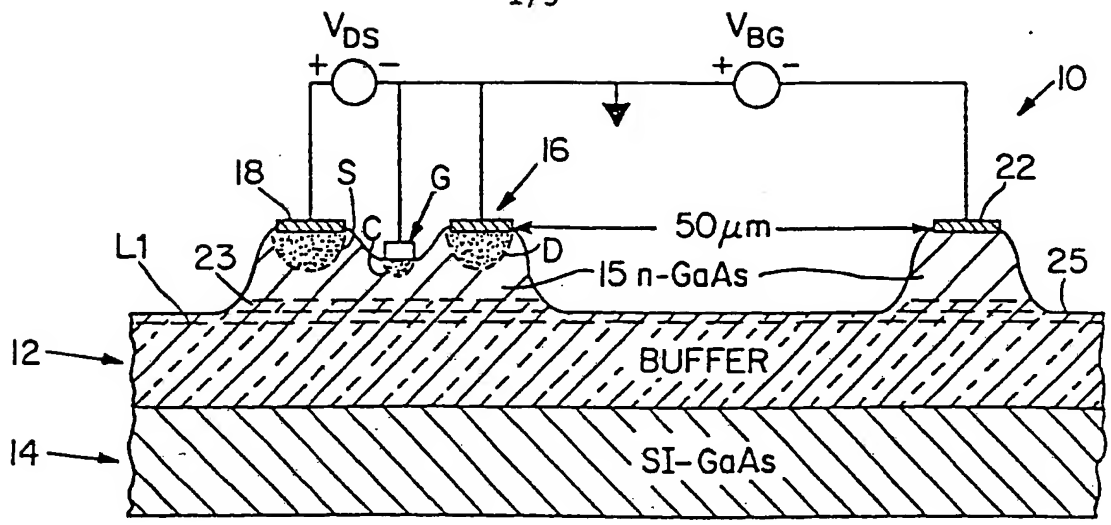
V_{DS}
V_{BG}
10
16
18
S
G
22
C
D
50μm
L1
23
15 n-GaAs
25
12
BUFFER
14
SI-GaAs

Fig. 1

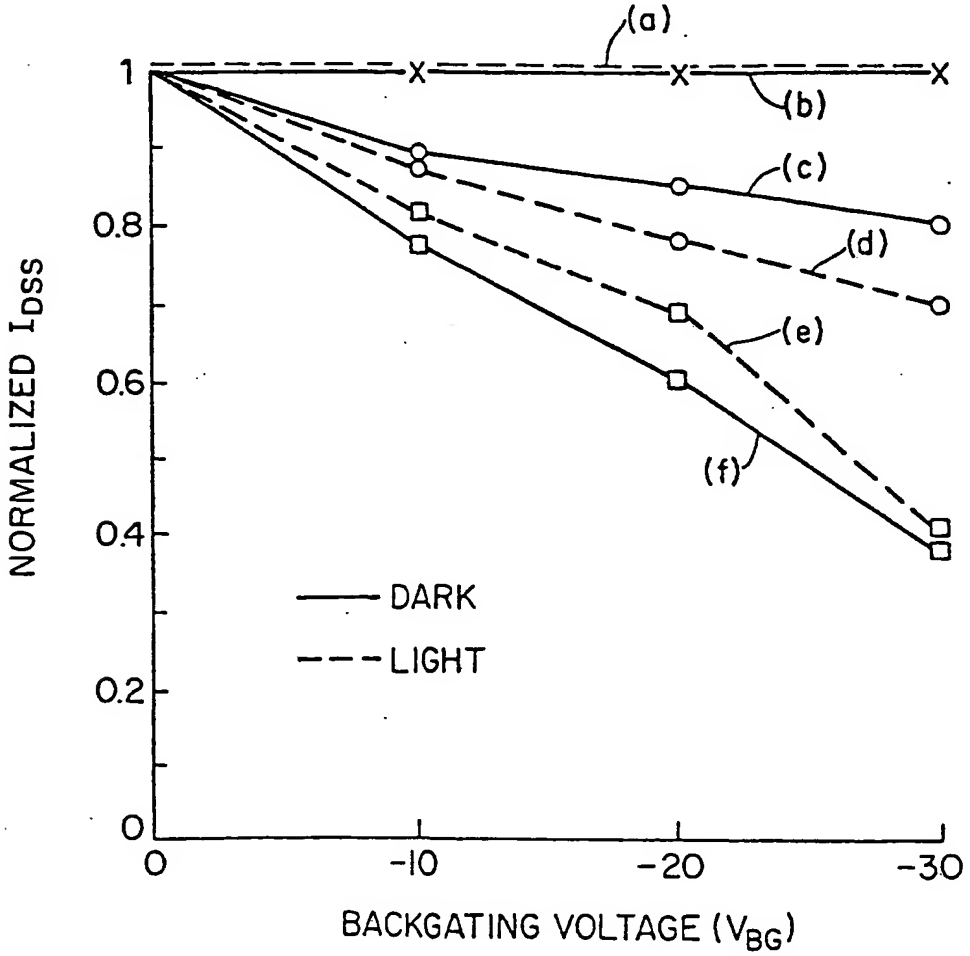
(a)
(b)
(c)
(d)
(e)
(f)
1
0.8
0.6
0.4
0.2
0
NORMALIZED I_{DSS}
DARK
LIGHT
0
-10
-20
-30
BACKGATING VOLTAGE (V_{BG})

Fig. 2

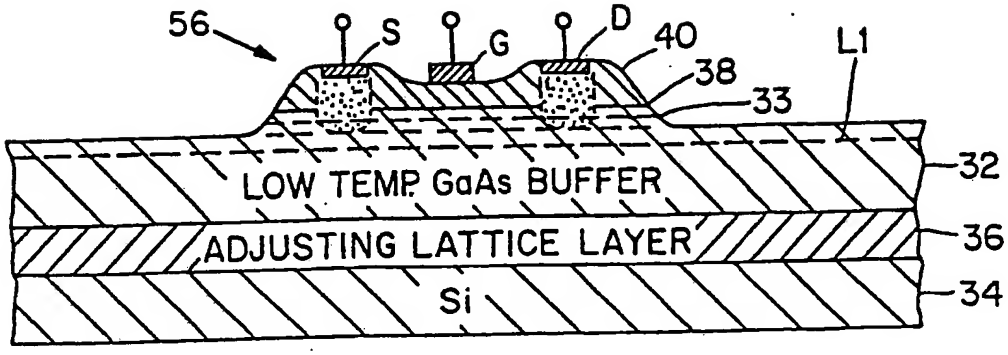

Fig. 3

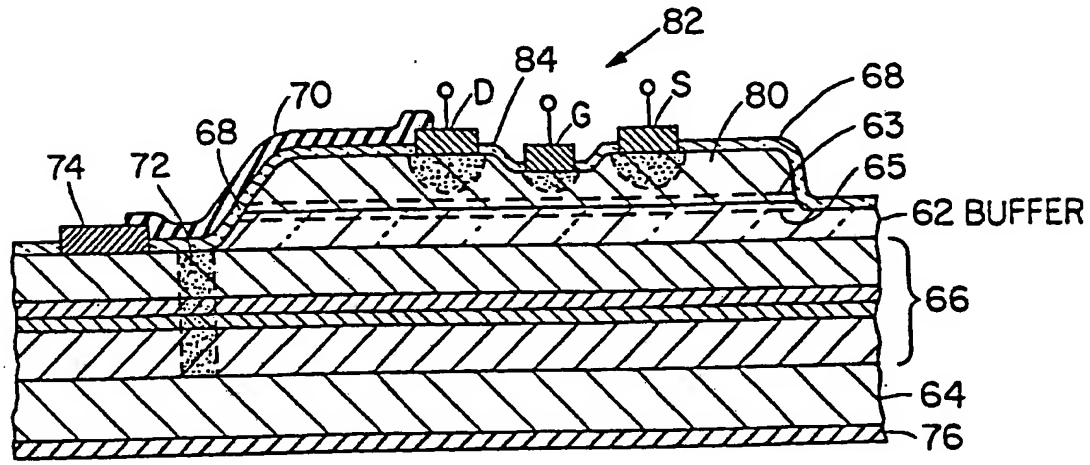

Fig. 4

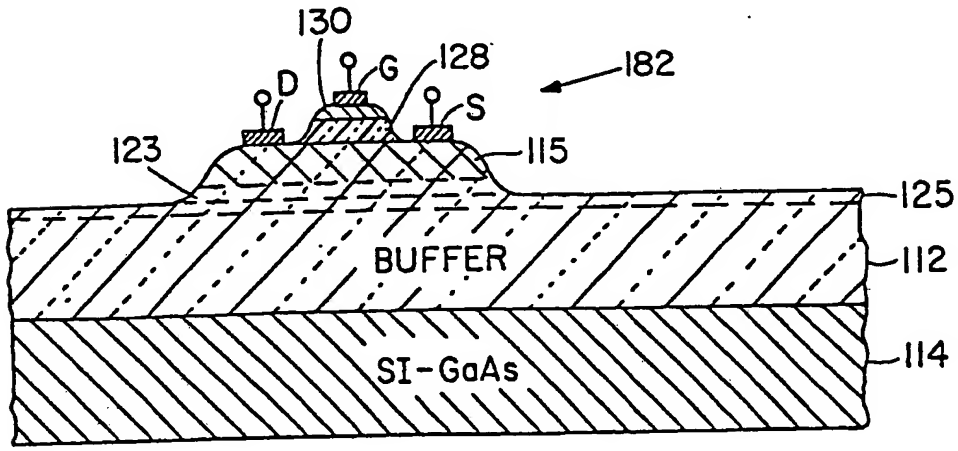

Fig. 5

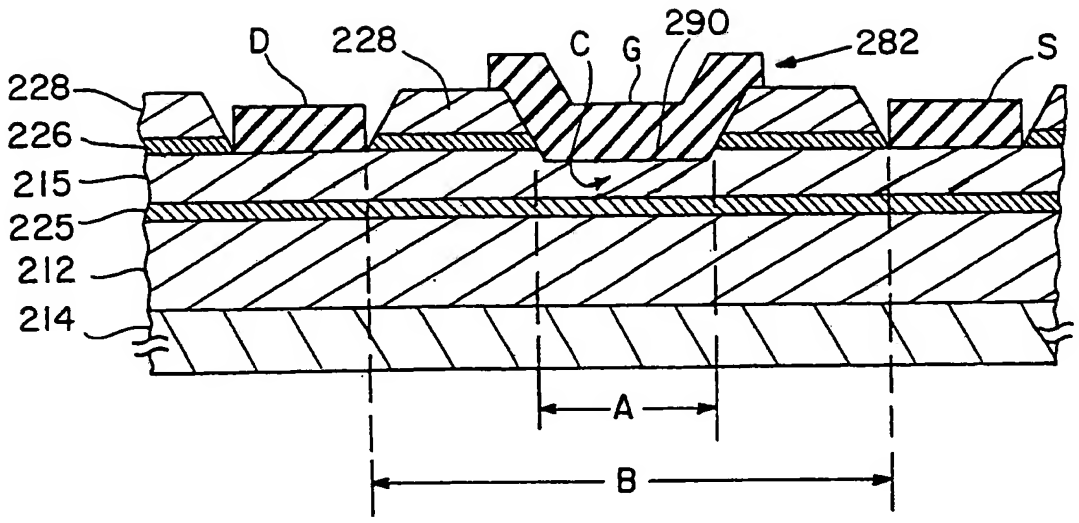

Fig. 6

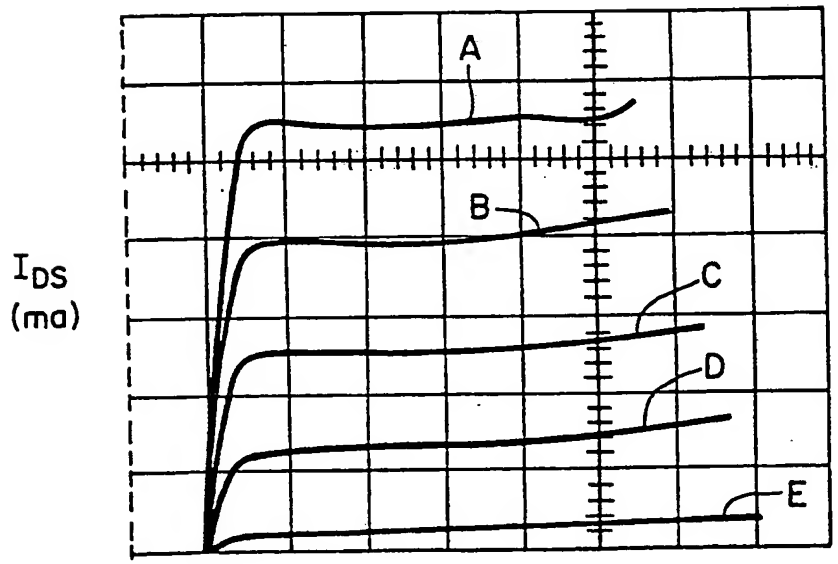

Fig. 7

INTERNATIONAL SEARCH REPORT

International Application No PCT/US 93/04383

I. CLASSIFICATION OF SUBJECT MATTER (if several classification symbols apply, indicate all)[6]

According to International Patent Classification (IPC) or to both National Classification and IPC

Int.Cl. 5 H01L29/10; H01L29/812; H01L27/15; H01S3/103
H01L21/82; H01L29/40; H01L21/338; H01L23/552

II. FIELDS SEARCHED

Minimum Documentation Searched[7]

Classification System	Classification Symbols
Int.Cl. 5	H01L

Documentation Searched other than Minimum Documentation to the Extent that such Documents are Included in the Fields Searched[8]

III. DOCUMENTS CONSIDERED TO BE RELEVANT[9]

Category °	Citation of Document,[11] with indication, where appropriate, of the relevant passages[12]	Relevant to Claim No.[13]
Y	WO,A,8 907 833 (MASSACHUSETTS INSTITUTE OF TECHNOLOGY) 24 August 1989	1-3, 13-15
A	see claim 1; figures 3,13	10

Y	IEEE ELECTRON DEVICE LETTERS vol. 12, no. 6, June 1991, NEW YORK US pages 306 - 308 , XP204424 C-L CHEN ET AL 'High Power density GaAs MISFET's with a low temparature grown epitaxial layer as the insulator' cited in the application	1-3, 13-15
Y	see the whole document	4,5,8, 11,12
A		17,19, 20,21,23

	-/--	

° Special categories of cited documents : [10]

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

IV. CERTIFICATION

Date of the Actual Completion of the International Search	Date of Mailing of this International Search Report
23 AUGUST 1993	08. 09. 93
International Searching Authority	**Signature of Authorized Officer**
EUROPEAN PATENT OFFICE	GELEBART J.F.M.

III. DOCUMENTS CONSIDERED TO BE RELEVANT (CONTINUED FROM THE SECOND SHEET)

Category °	Citation of Document, with indication, where appropriate, of the relevant passages	Relevant to Claim No.
Y	INTERNATIONAL ELECTRON DEVICES MEETING, December 1988, IEEE, NEW-YORK, US pages 838 - 841 F.W. SMITH ET AL 'Sidegating reduction for GaAs integrated circuits by using a new buffer layer'	4,5,8, 11,12
A	see page 838, right column - page 839, left column	1,17,20, 21
A	EP,A,0 022 383 (THOMSON-CSF) 14 January 1981 see page 3, line 2 - page 3, line 14; figures 1-10	17,18, 20-23
A	APPLIED PHYSICS LETTERS vol. 57, no. 24, 10 December 1990, NEW YORK US pages 2570 - 2572 D.C. LOOK ET AL 'Unpinning of GaAs surface Fermi level by 200 degrees C molecular beam epitaxial layer' see page 2570, right column	17,18, 20-23
A	EP,A,0 124 256 (FUJITSU LTD.) 7 November 1984 see page 6, line 11 - page 17, line 23; figures 24-27,30,31	6,7,17, 21
A	IEEE ELECTRON DEVICE LETTERS vol. 11, no. 12, December 1990, NEW YORK US pages 561 - 563 , XP160779 L.-W. YIN ET AL 'Improved breakdown voltage in GaAs MESFET's utilizing surface layers of GaAs grown at low temperature by MBE' see page 562, left column	17,20-23
A	IEEE ELECTRON DEVICE LETTERS vol. 10, no. 12, December 1989, NEW YORK US pages 565 - 567 , XP87811 A.S. BROWN ET AL 'AlInAs-GaInAs HEMT's utilizing low temprature AlInAs buffers grown by MBE'	1,16
A	NTIS TECH NOTES October 1990, SPRINGFIELD, VA US page 823 , XP171436 'AlAs diffusion/Schottky barriers on GaAs' see page 823	

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III. DOCUMENTS CONSIDERED TO BE RELEVANT (CONTINUED FROM THE SECOND SHEET)

Category °	Citation of Document, with indication, where appropriate, of the relevant passages	Relevant to Claim No.
P,X	IEEE ELECTRON DEVICE LETTERS vol. 13, no. 6, June 1992, NEW YORK US pages 335 - 337 C-L CHEN ET AL 'Hogh-breakdown voltage MESFET with a low temperature grown GaAs passivation layer and overlapping gate structure' see figure 1	1,3-9, 11-15, 17-23

ANNEX TO THE INTERNATIONAL SEARCH REPORT ON INTERNATIONAL PATENT APPLICATION NO.

US 9304383
SA 74439

This annex lists the patent family members relating to the patent documents cited in the above-mentioned international search report. The members are as contained in the European Patent Office EDP file on 23/08/93
The European Patent Office is in no way liable for these particulars which are merely given for the purpose of information.

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
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		DE-A- 3471830	07-07-88